Status on SRS + Timepix

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Titel

- SRS + Timepix

- 96 Chip Module

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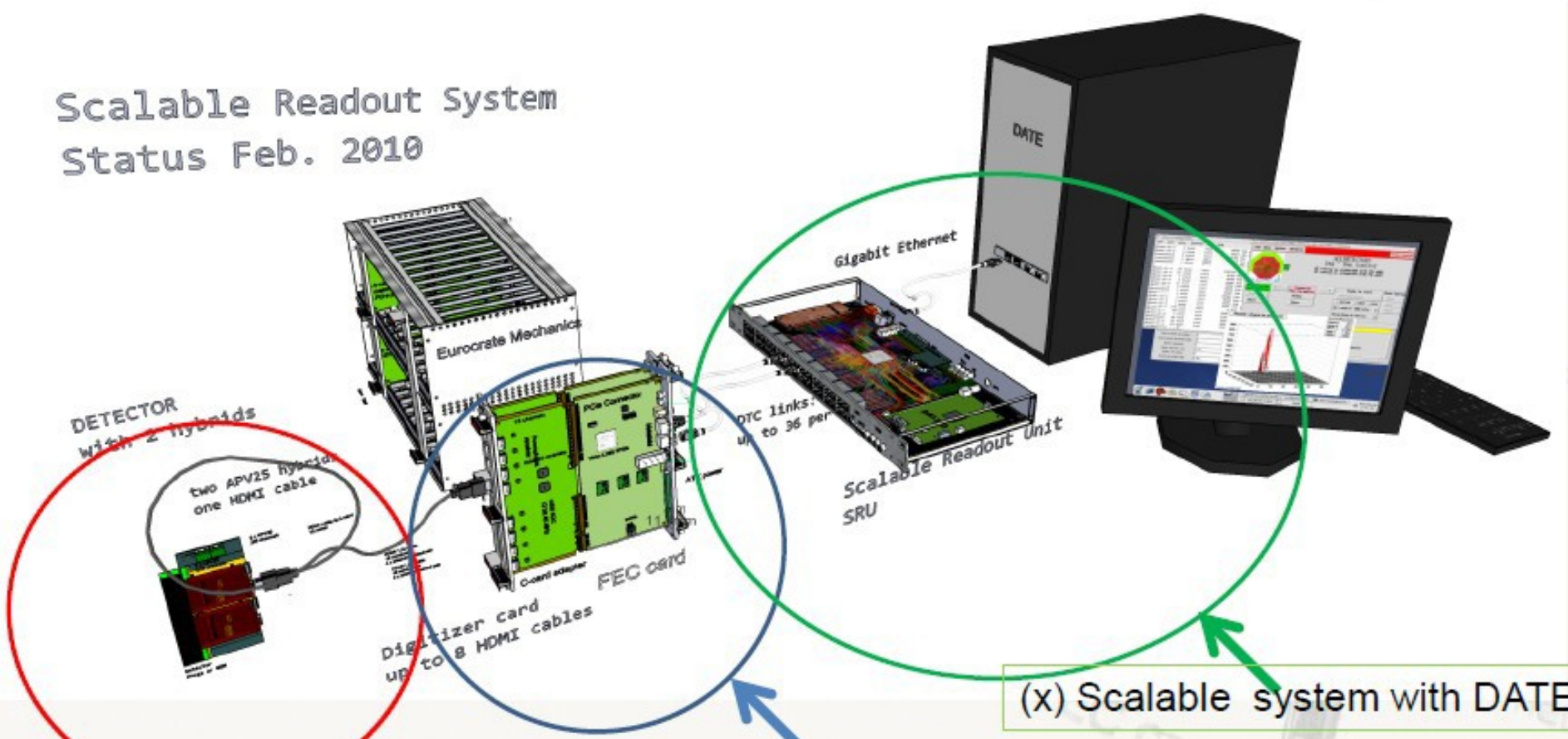
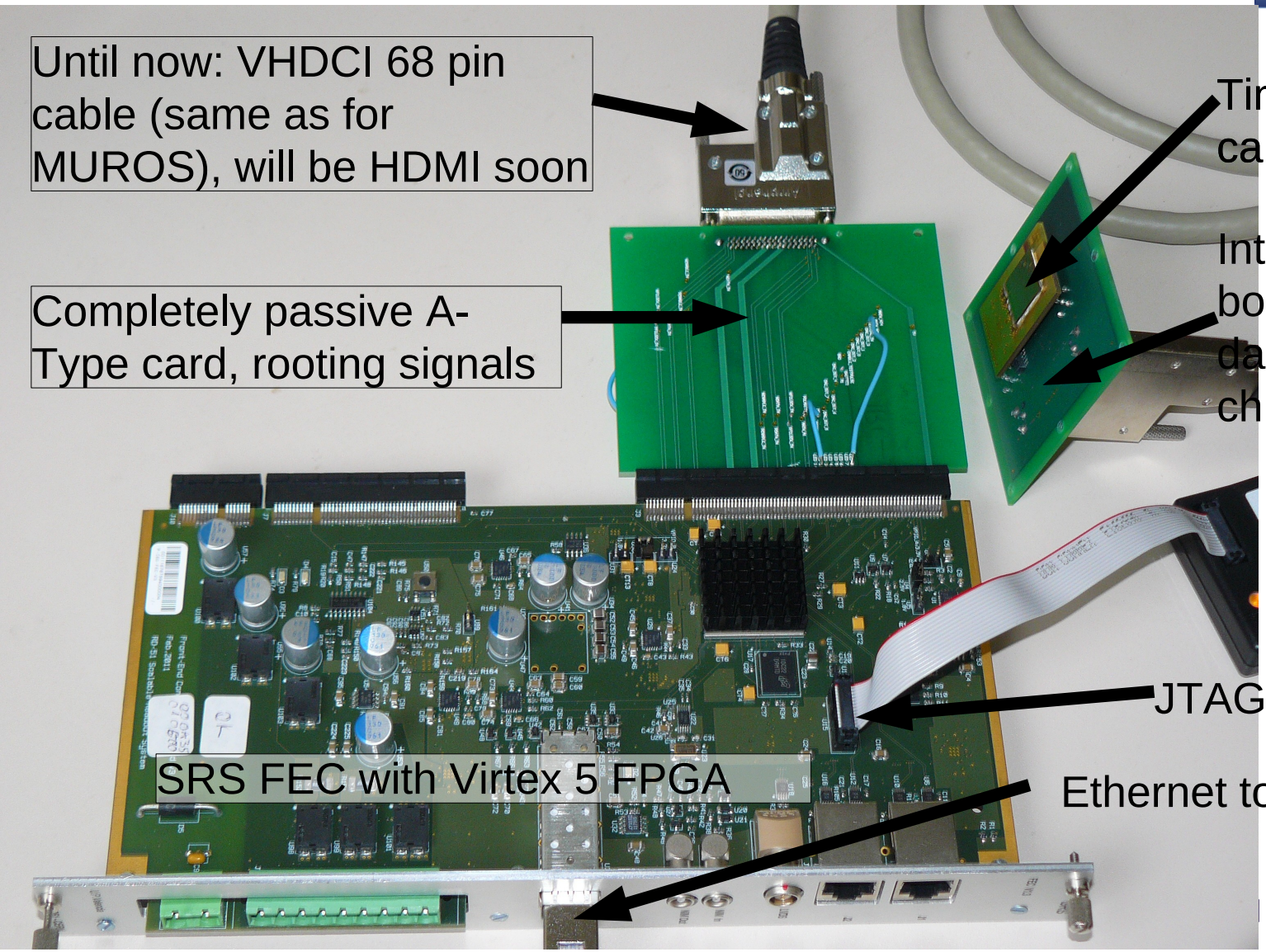
SRS

- Scalable Readout System (RD51, CERN)

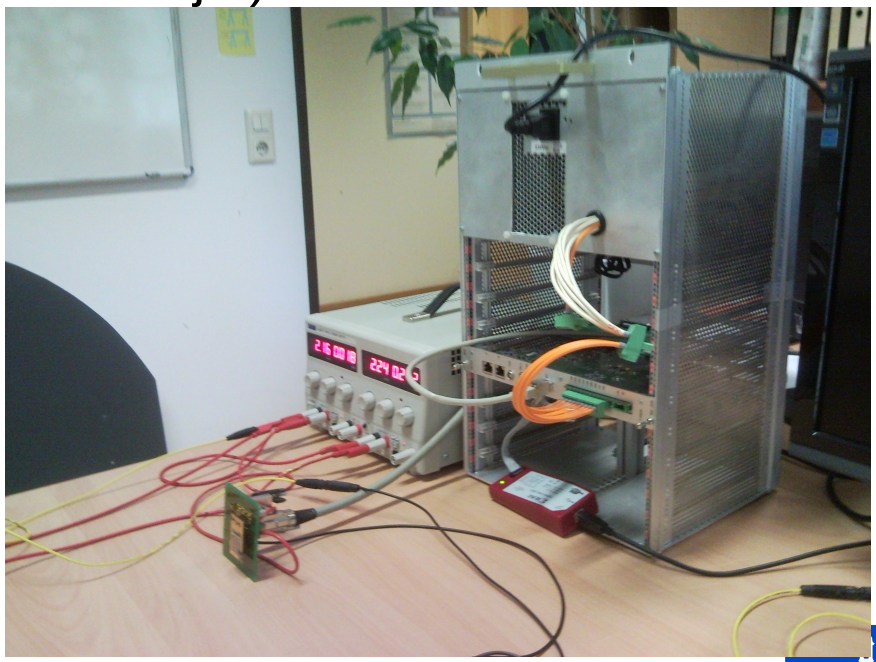


SRS with Timepix chip



Status Timepix+SRS Readout

- Most of the functionality of the Muros+Pixelman system is implemented
  - Set matrix and DACs (FSR)
  - Read out matrix
  - Reset, start/stop measurement, measure with certain shutter length
  - DAC scan in Software + osci (no ADC jet)
  - Threshold equalisation
  - External test pulses
- Setup with one chip in operation
- Octoboard production ongoing
- Software/Firmware modifications for octoboard



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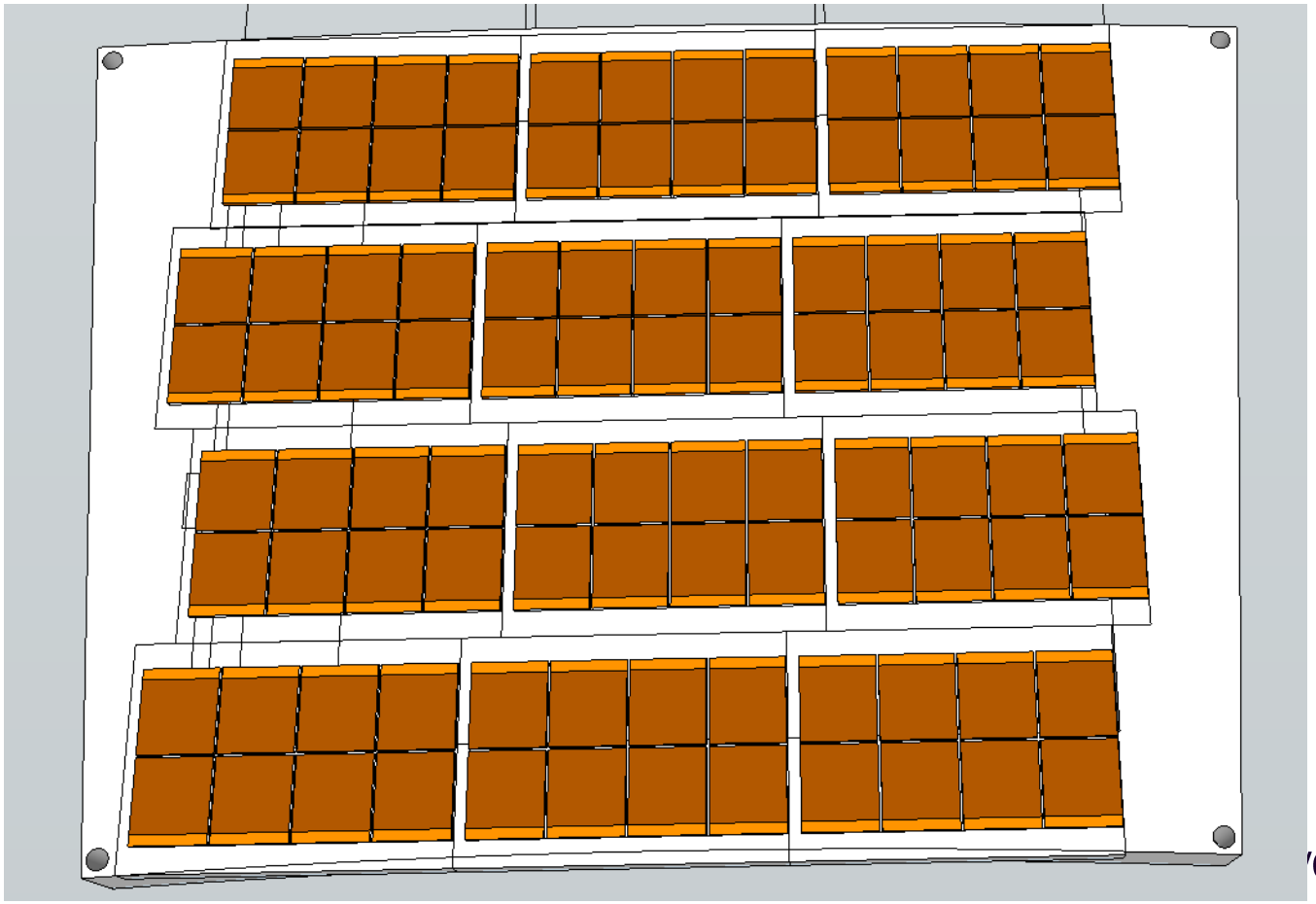
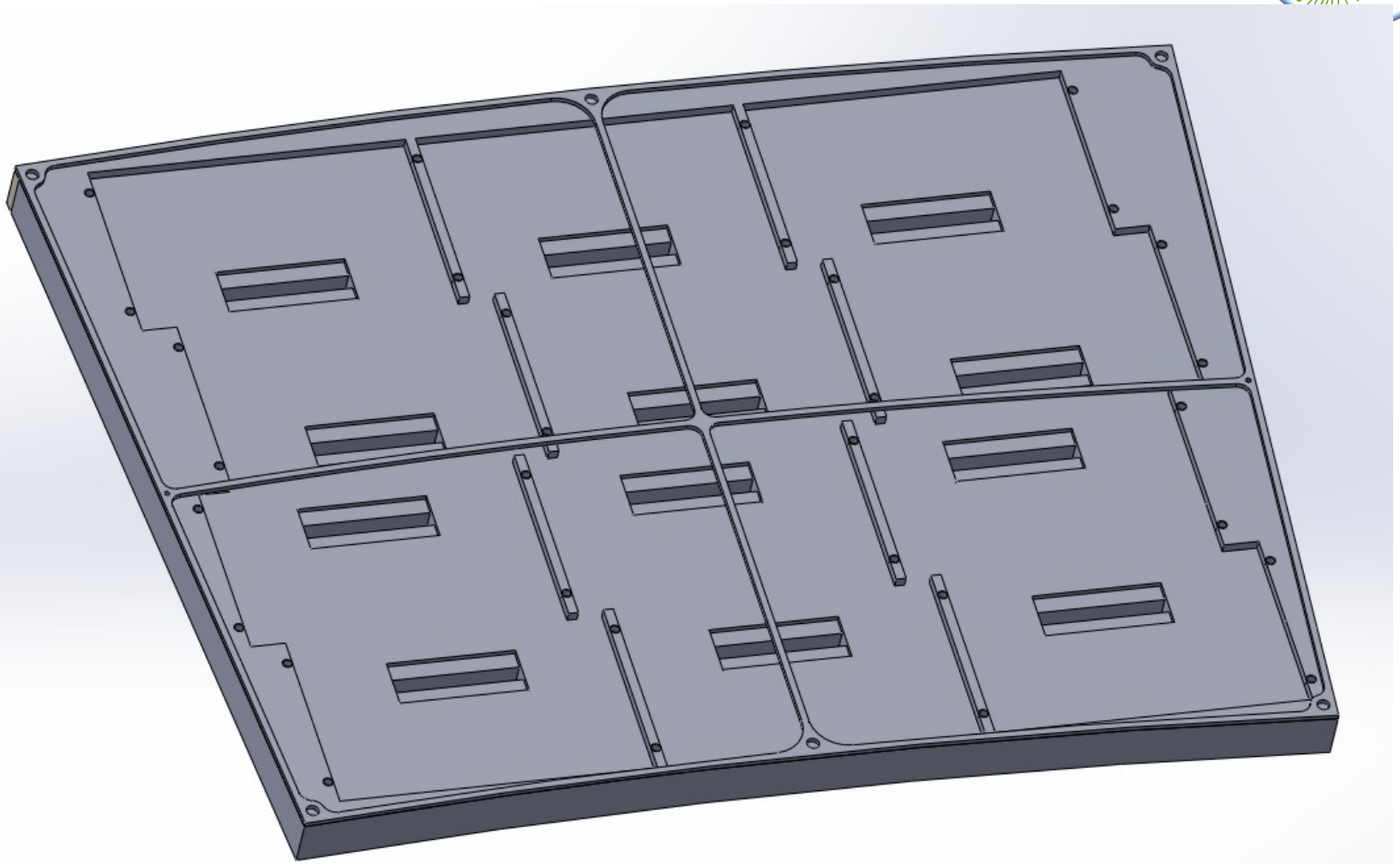
96 chip module

- Near goal: LCTPC module with 4x3 submodules, each octoboards, staggered boards



96 chip board



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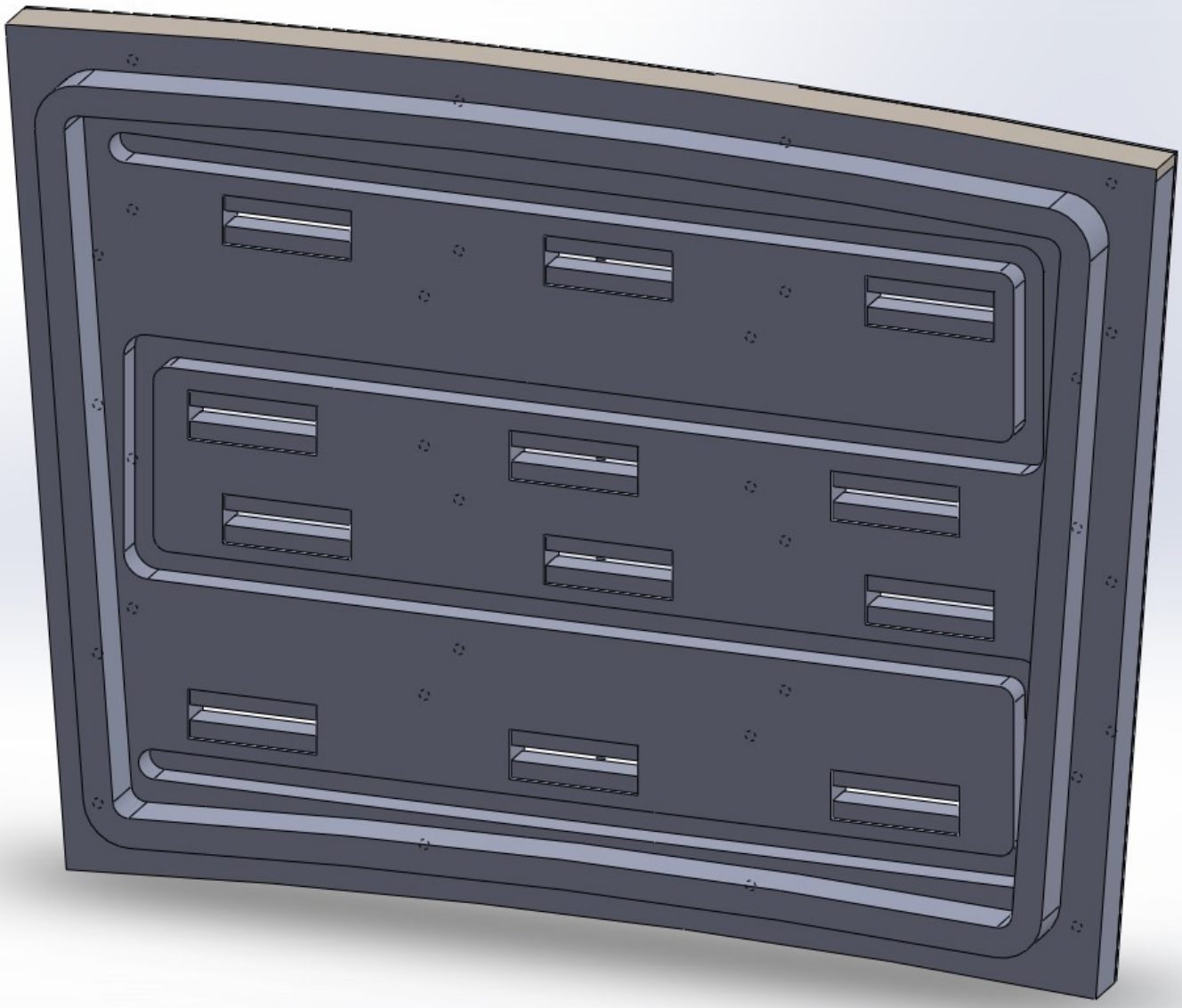
96 chip board



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Summery

Timepix chip is used as readout structure in gaseous detector (prototypes)

- SRS + Timepix in operation
- Data taking possible
- Software/Firmware extensions for octoboard in preparation
- Preparation of LCTPC module with O(100) chips
  - Hardware modifications on detector side planed
    - HDMI cables
    - Electronics
    - Power supply
  - Adapter card will also be modified
  - Cooling (Master student)

- First octoboard (Timepix chips) might be ready soon

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Motivation

Advanced European Infrastructures for Detectors at Accelerators
- 4 year EU FP 7 Research Infrastructures program project
- Started February 2011
- > 80 institutes from 23 European countries
- Budget: 27 million € (8 million € from the EU)
- Coordinated by CERN

Subtask 9.2.3 (Bonn, CEA, Mainz, NIKHEF):
Common readout systems for gaseous detectors. Auxiliary electronics for the read-out of pixellated front-end chips, aimed at highly granular pixel read-out of gas detectors, are to be developed.

→ New readout system for pixellated chip (Timepix chip)
→ Cover large area for TPC/inner tracker application

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People in AIDA Subtask 9.2.3

- Bonn:
  - Klaus Desch (Professor)
  - Jochen Kaminsky (PostDoc), new chip carrier, adapter card (SRS)
  - Michael Lupberger (PhD), FPGA firmware on Virtex6/SRS
- CEA:
  - Paul Colas (group leader)
  - Technicians at CEA, supporting hardware for chip carier
- ~~Mainz:~~
  - ~~Uli Schäfer (Dr.)~~
  - ~~Christian Kahra in some time as PhD (?), PC software~~
  - ~~Michael Zamrowski (gone), 1st version of FPGA on Virtex5~~
- NIKHEF
  -
- CERN: support from SRS group
  - Hans Müller (coordinater), Sorin, Jose (FEC design)

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