GOSSIPO 3

A front-end pixel chip prototype for read-out of MPGDs

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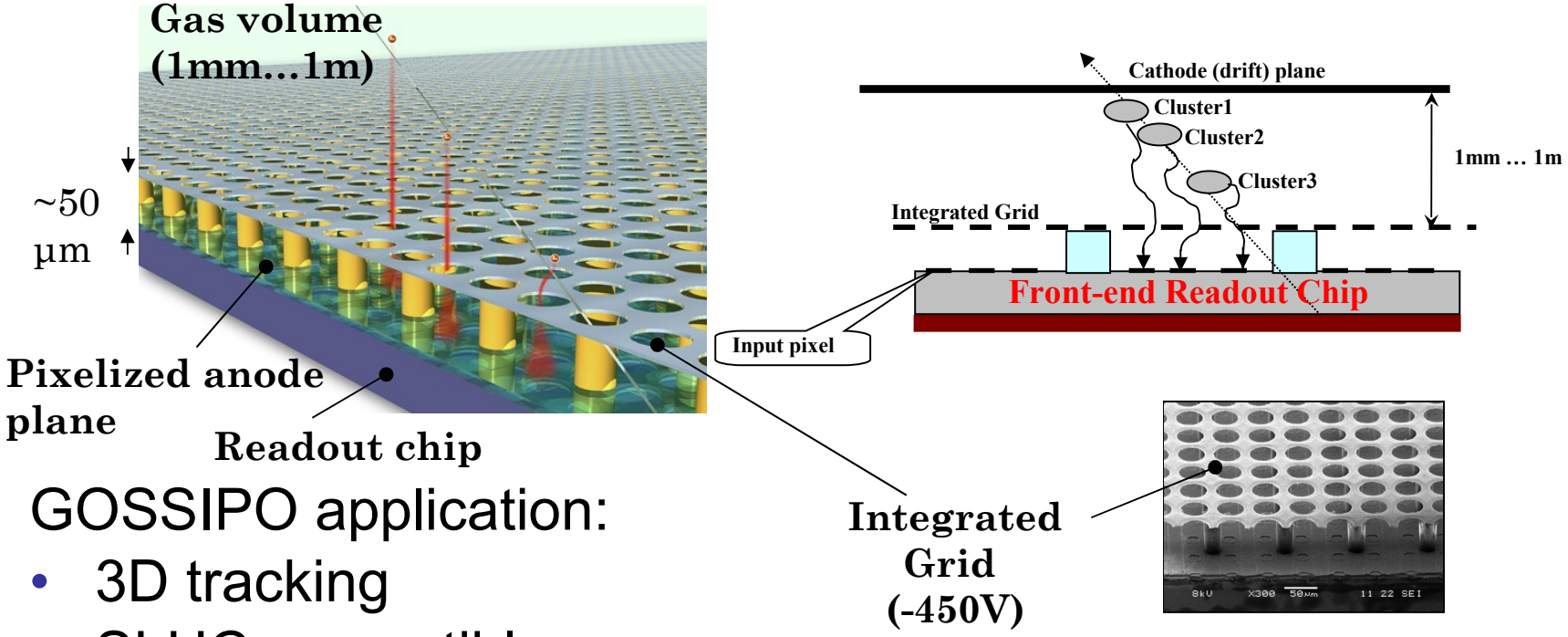
MPGD read-out



GOSSIPO application:

- 3D tracking
- SLHC compatible
- High efficiency of detection of single primary electrons
- High resolution TDC (each pixel)
- Low power

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GOSSIPO3: Goals

- Prototype should lead to a chip with:
  - Pixel size ~ 60 x 60 μm²
  - Accuracy (bin size of TDC) ~1.7ns
  - Drifttime up to 100μs
  - ToT accuracy ~ 200e^- (~ 27ns)
  - ToT up to 6.4μs (~ 28ke^-)
  - Noise ~ 70e^-
  - Rise time 20ns
  - Power consumption < 100mW/cm² (~ 3μW/ch)
- Features will be:
  - One of two modes: Time measurement or counting
  - Timemode allows: Hit arrival time & ToT in each pixel simultaneously
  - External trigger
  - First steps towards selftriggering (fast OR from InGrid)

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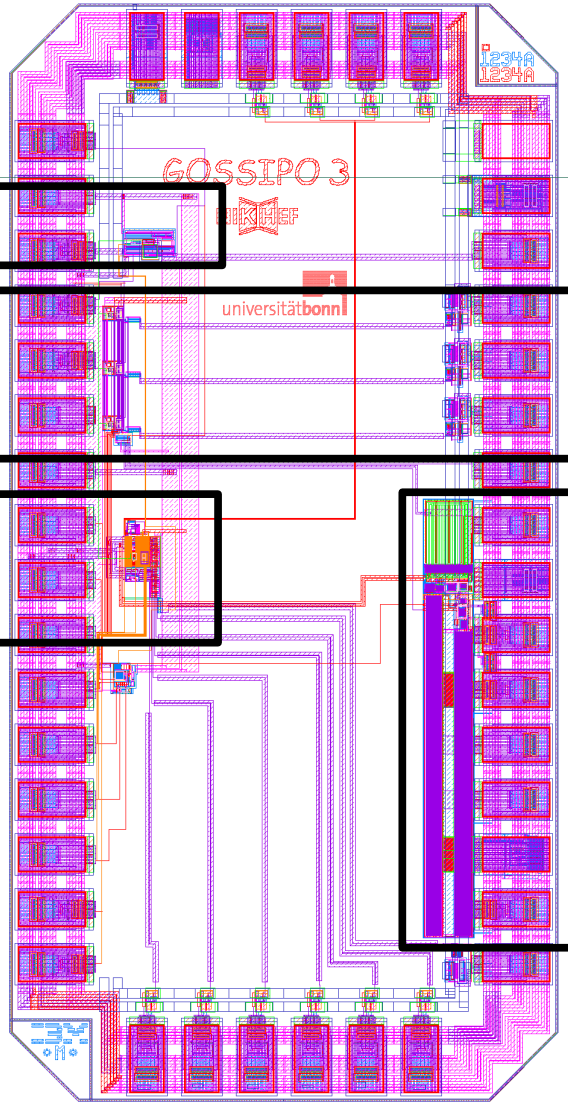
MPW run on 21.09.09

InGrid preamp

Analogue signal chain
(3 preamps & comparators)

Two complete Pixels
(one without front-end)



LDO (vddd)

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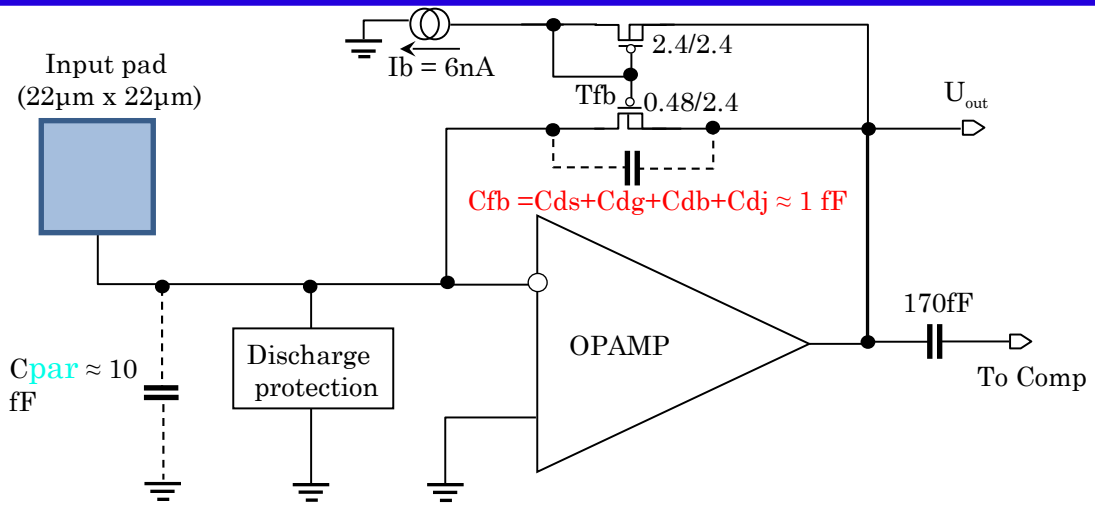
Front-end



- Low parasitic capacitance (10fF)
- Very small feedback capacitor therefore high gain
- Constant current feedback (1nA)
- Low power consumption (3µW/ch)
- Low noise (70e^-)
- Channel to channel threshold spread ~ 70e^-

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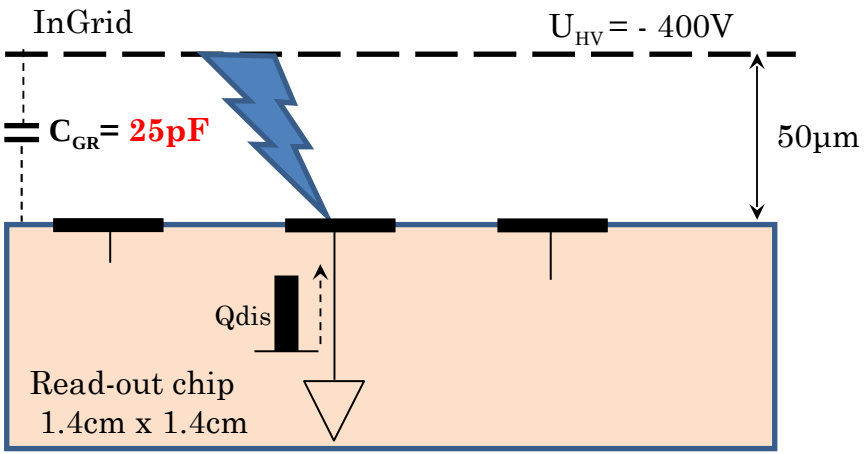
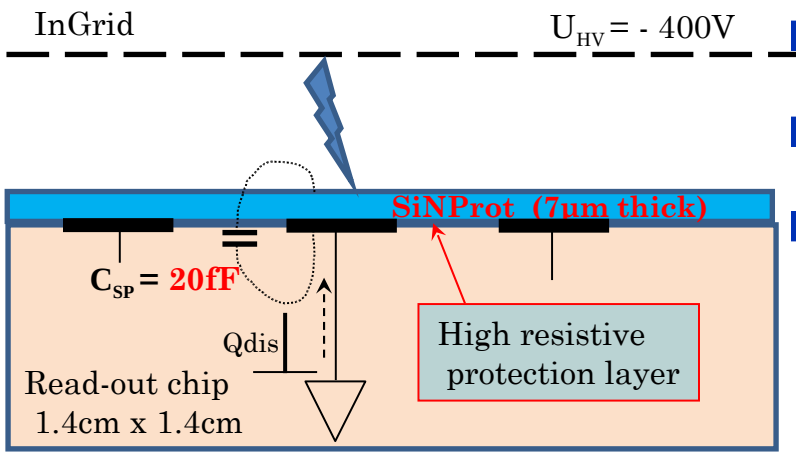
Discharge protection

NO protection layer



$Q_{dis} = U_{HV} \bullet C_{GR} = 10\ 000pC$

With protection layer



$Q_{dis} = U_{HV} \bullet C_{SP} = 8pC$

SiNProt layer limits the size the discharge

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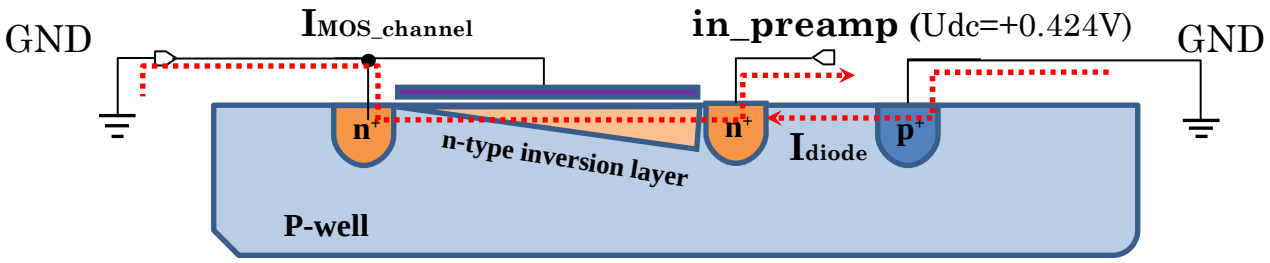
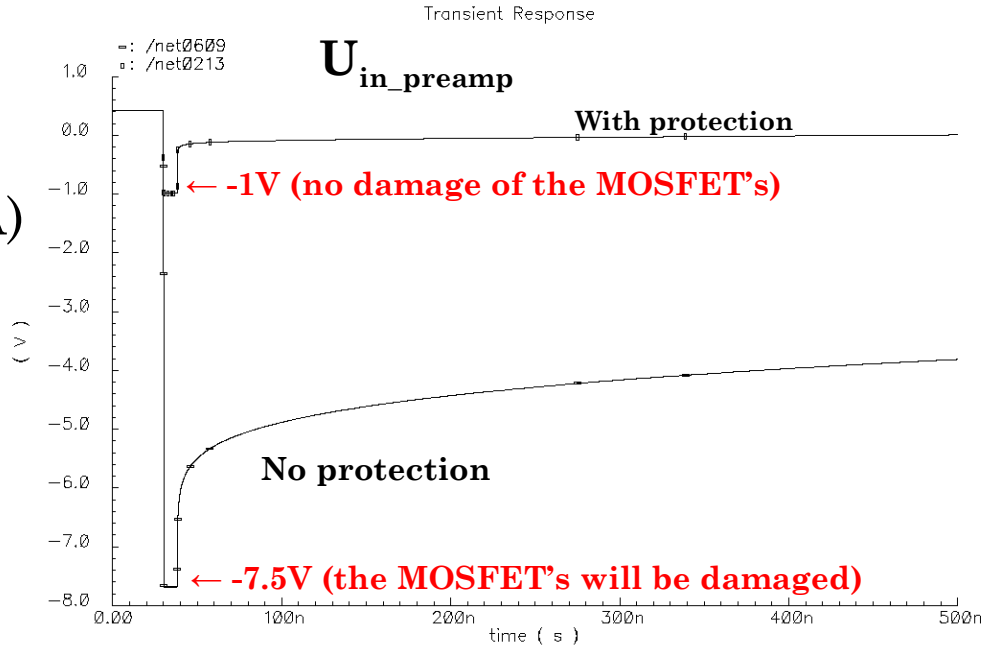
Protection device

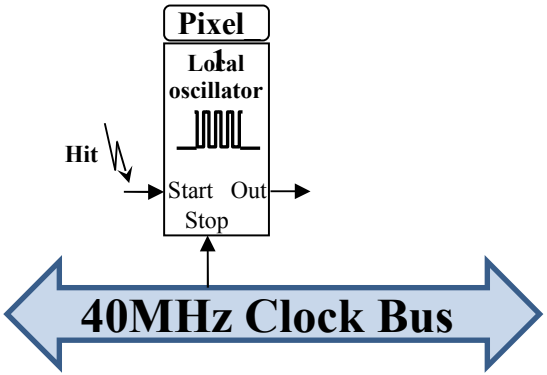
Standard NFET (W=1µm, L=0.24 µm)

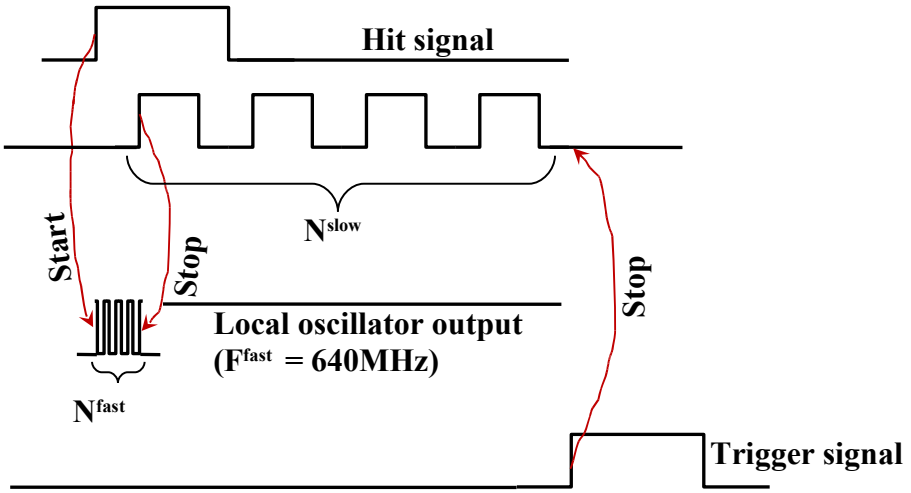


- Small area (w=1µm l=0.24µm)
- Low parasitic capacitance (1.3fF)
- Negligible leakage current (250pA)

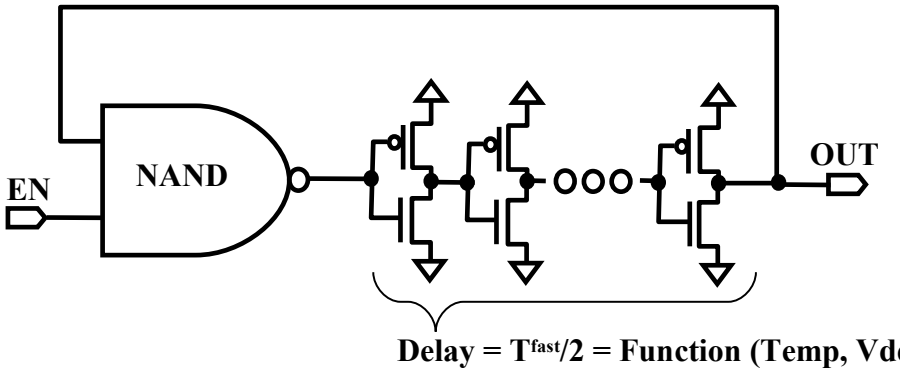


TDC with Local fast oscillator





- Time = $N^{slow} / F^{slow} + N^{fast} / F^{fast}$
- Eliminates need for a fast clocknet, reducing:
  - Power needs (relaxed demands to clock buffers & smaller effect of parasitcs)
  - Crosstalk



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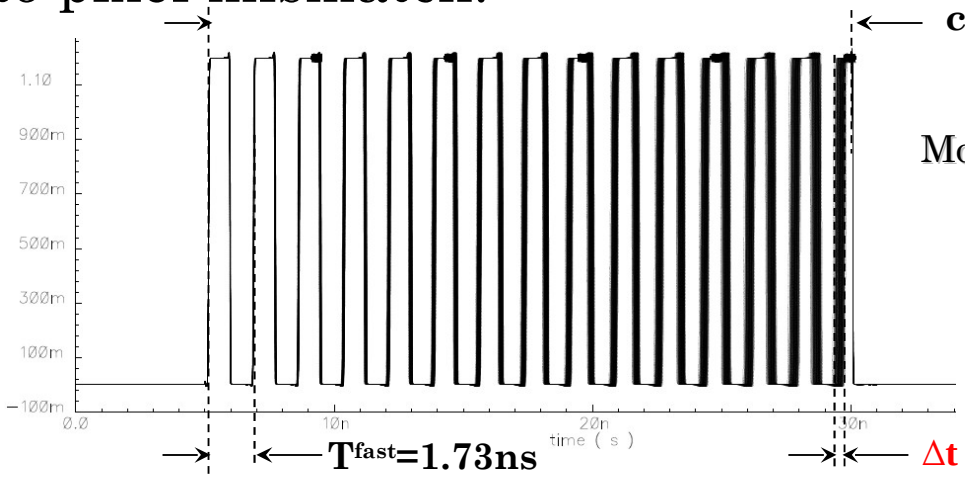
Matching issues

- Pixel to pixel mismatch:



Monte Carlo simulations.

- Process variation (wafer to wafer mismatch)

vdd_osc	nominal	lower limit	upper limit
0.61 V		1.72 ns	
0.76 V	1.73 ns	1.13 ns	2.26ns
1.1 V			1.72 ns

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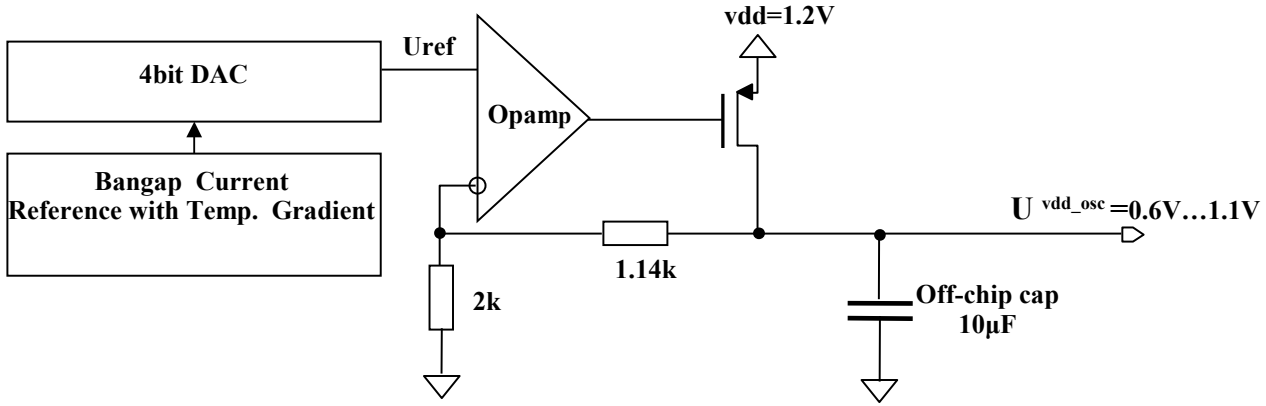
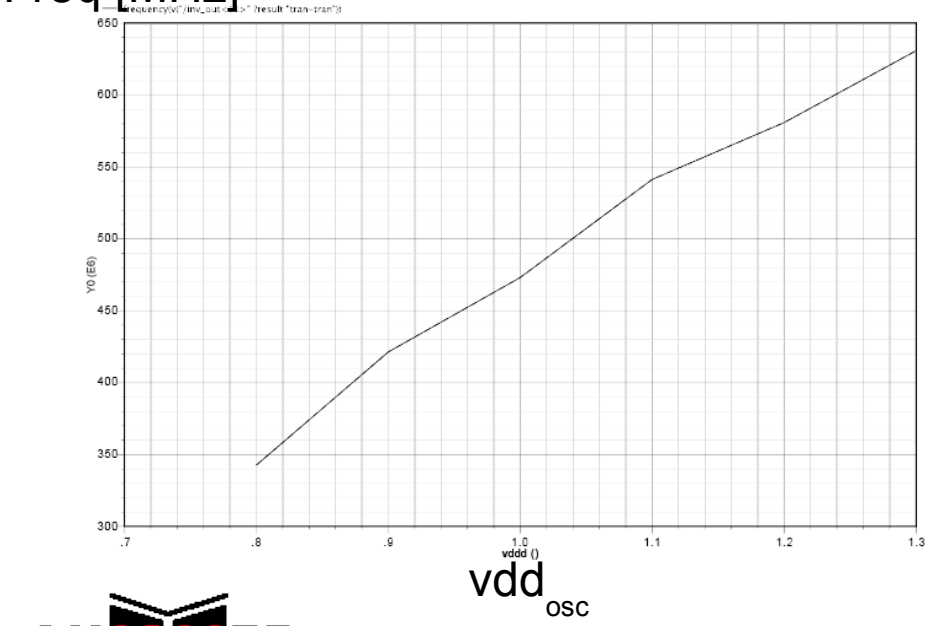
Onchip LDO





- VDD adjustment allows frequency tuning for all fast oscillators on the chip
  - This can compensate die to die frequency mismatch
  - Pixel to Pixel mismatch is negligible (no Pixel tuning needed)
  - Temperature effects may be compensated via reference voltage

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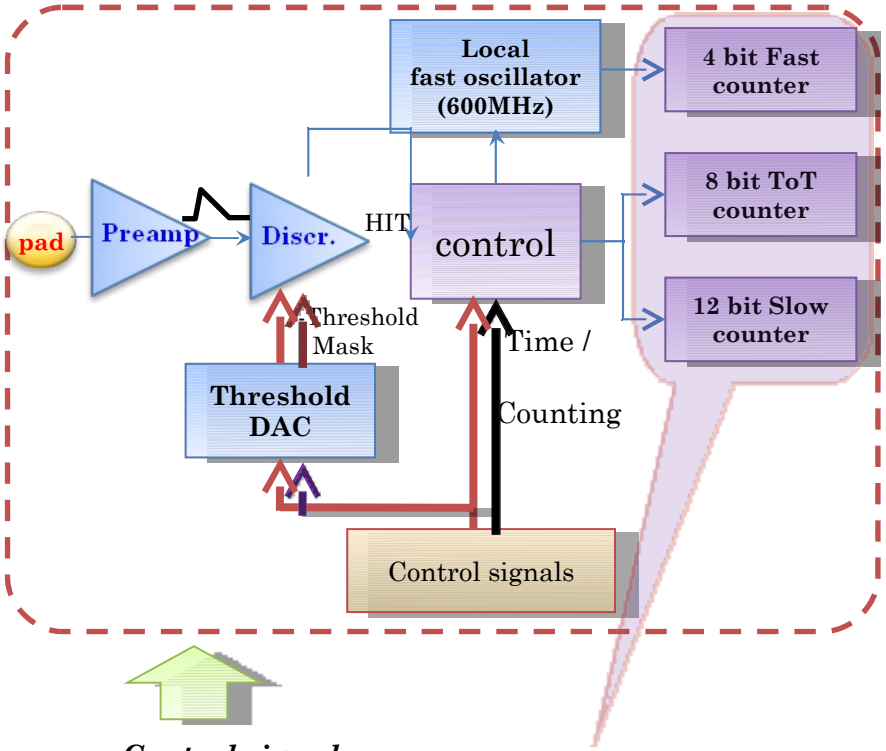
The Pixel

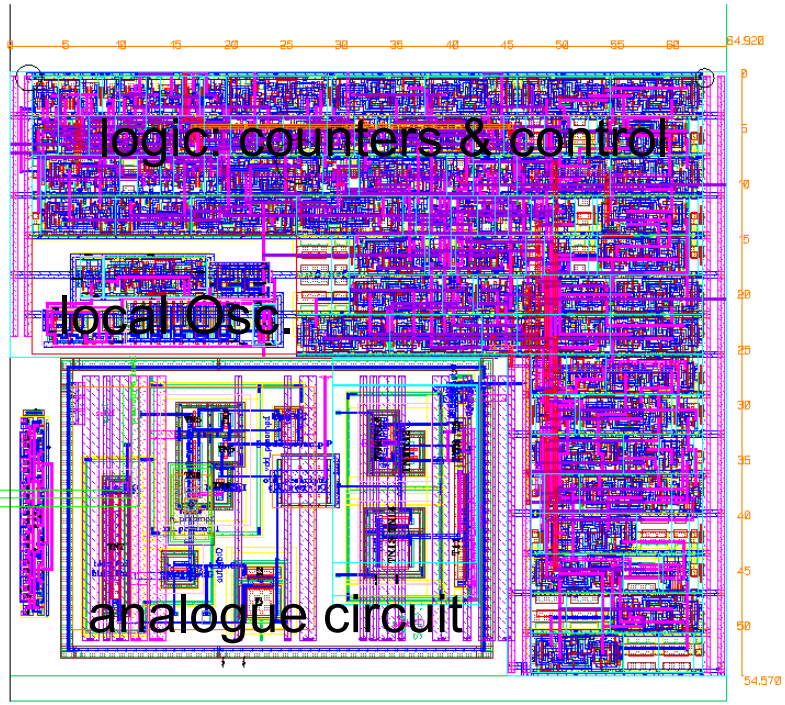
Block diagram



Control signals
- *Slow clock*
- *TRIGGER (common stop)*
- *TOKEN*
- *RESET*

LFSR = Counters (data taking) or LFSR = Shift registers (data read-out)

Layout



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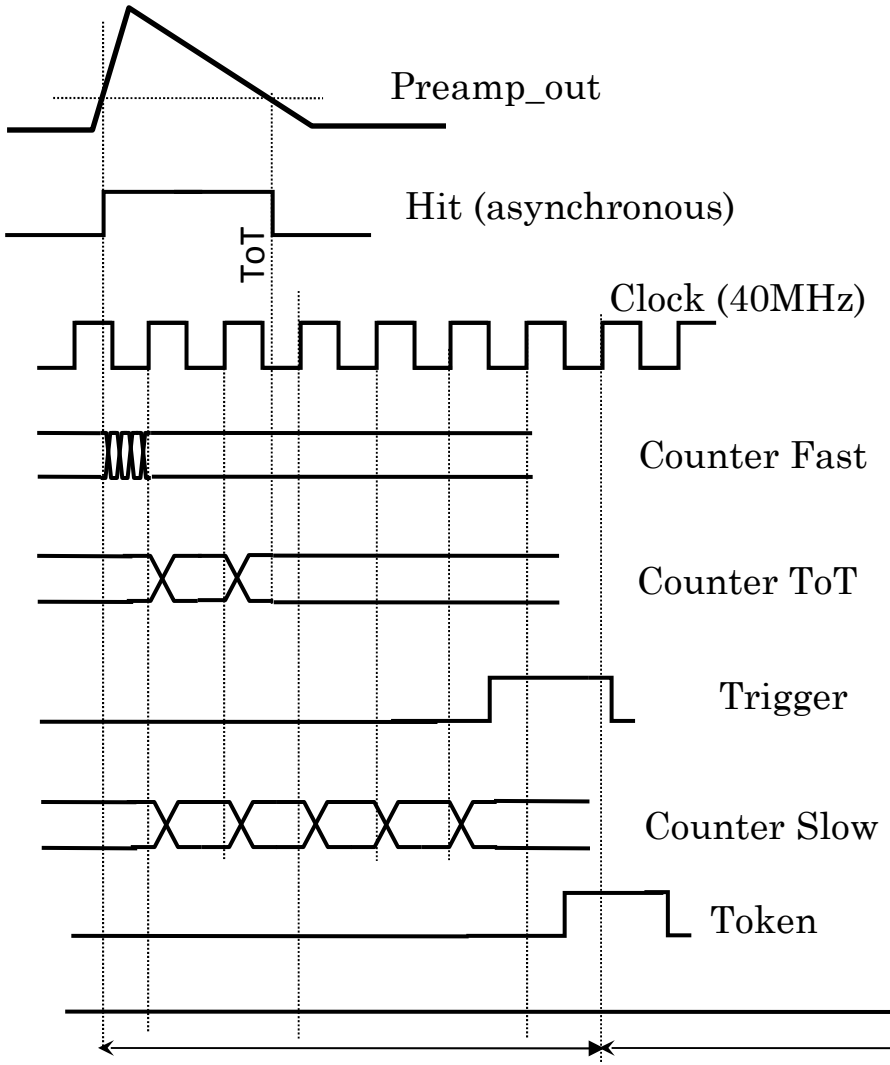
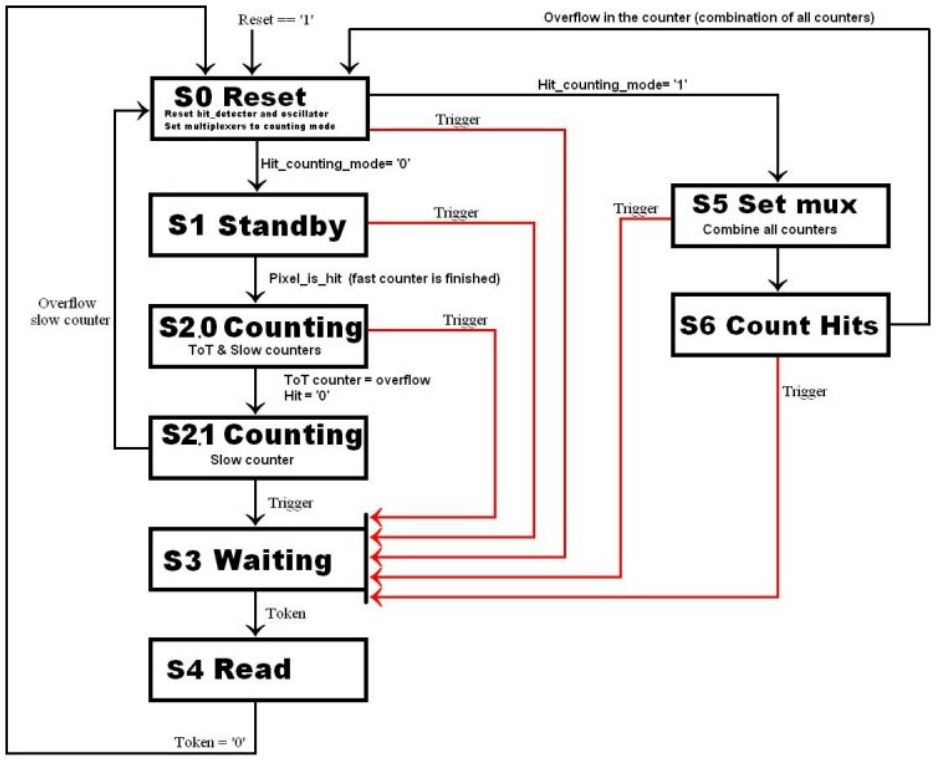
Pixel Logic


Preamp_out
Hit (asynchronous)
ToT
Clock (40MHz)
Counter Fast
Counter ToT
Trigger
Counter Slow
Token
Reset
Data taking phase (LFSR = Counter)
Data read-out Phase (LFSR = Shift Registers)


Reset == '1'
Overflow in the counter (combination of all counters)
S0 Reset
Reset hit_detector and oscillator
Set multiplexers to counting mode
Hit_counting_mode= '1'
Trigger
Hit_counting_mode= '0'
S1 Standby
Trigger
Trigger
S5 Set mux
Combine all counters
Pixel_is_hit (fast counter is finished)
Overflow slow counter
S2.0 Counting
ToT & Slow counters
Trigger
S6 Count Hits
ToT counter = overflow
Hit = '0'
Trigger
S2.1 Counting
Slow counter
Trigger
S3 Waiting
Token
S4 Read
Token = '0'

Conclusions

- GOSSIPO-3 is a prototype chip of a front-end pixel chip for read out of MPGDs
- Every pixel features:
  - A high resolution TDC (1.7ns)
  - Dynamic range up to 100µs
  - A ToT counter
- As the chip itself the testsystem is developed by NIKHEF and Bonn in close collaboration

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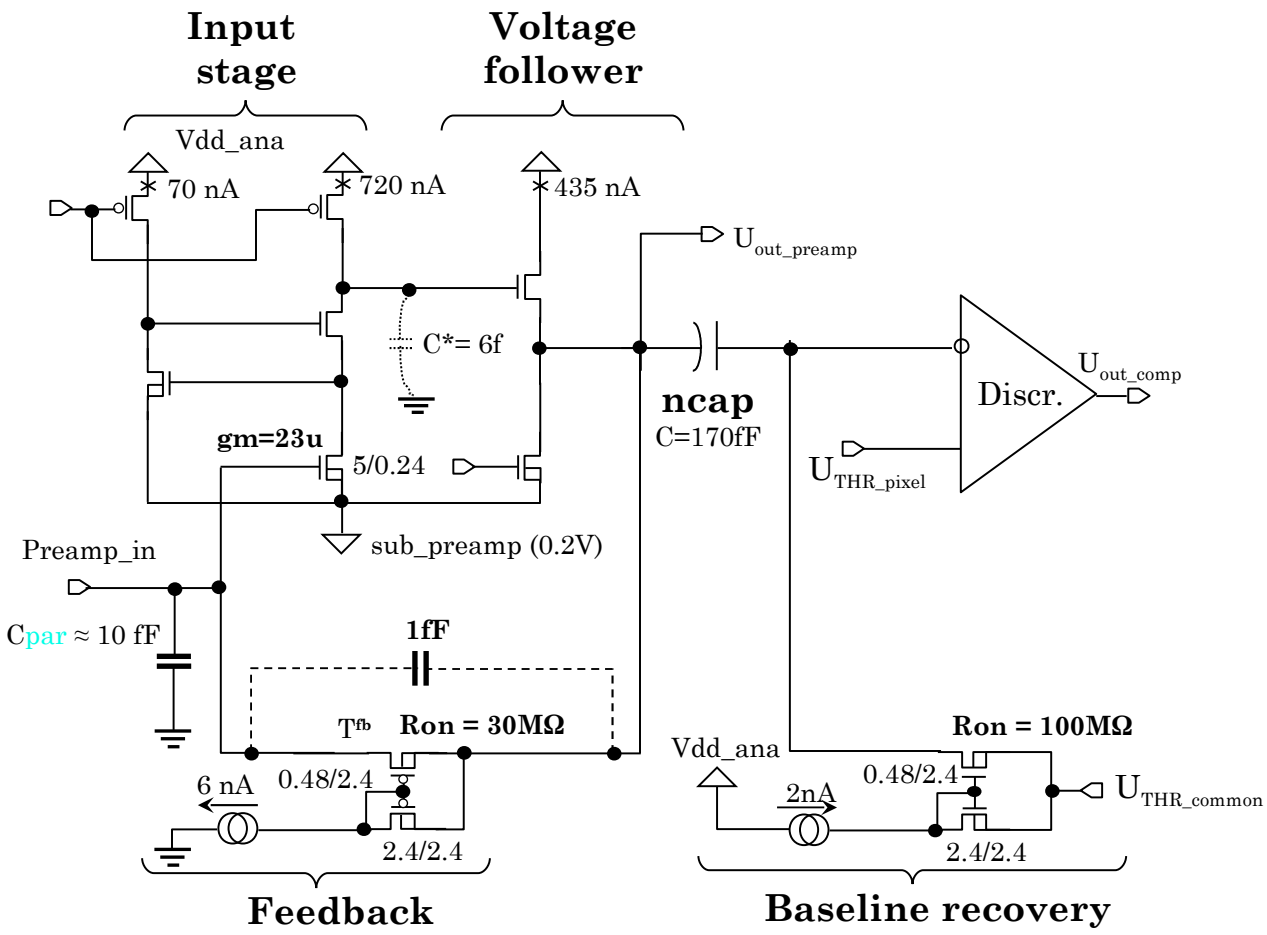
The front-end circuit



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